PRELIMINARY

RFuW Engineering Pte. Ltd.

RFLM-502602QA-TBD

Quasi-Active C Band Limiter Module

Features:

- Frequency Range: 5.0 GHz to 6.0 GHz
- Peak Power: +62 dBm
- Average Power: +56 dBm
- Insertion Loss: <1.2 dB
- Return Loss: >13 dB
- Flat Leakage Power: <21 dBm
- Spike Energy Leakage: <0.5 ergs
- Surface Mount Limiter Module: TBD
- Optional DC Coupling Capacitors
- No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-502602QA-TBD SMT Silicon PIN Diode Limiter Module offer both High Peak Power and High Average Power protection in the 5.0 GHz to 6.0 GHz frequency range. It is based on proven hybrid assembly techniques utilized extensively in high reliability, mission critical applications. The RFLM-502602QA-TBD offers excellent thermal characteristics in a compact, SMT package. The RFLM-502602QA-TBD is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the 5.0 GHz to 6.0 GHz frequency range.

The RFLM-502602QA-TBD Limiter Module provides outstanding passive receiver protection (always on) which protects against High Peak Power up to +62 dBm pulsed and High Average Power up to +56 dBm while maintaining low flat leakage to less than +21 dBm, and reduces Spike Leakage to less than 0.5 ergs.

ESD and Moisture Sensitivity Rating

The RFLM-502602QA-TBD Limiter Module carries a Class 1 ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The RFLM-502602QA-TBD based substrate has been design to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. Also, a proprietary

design methodology has minimized the thermal resistance from the PIN Diode junction to base plate (R_{THJ-A}). This circuit topology coupled with the thermal characteristic of the substrate design enables reliably handling High Input RF Power up to +56 dBm CW and RF Peak Power levels up to +62 dBm (150 uSec pulse width @ 10% duty cycle with base plate temperature at +55°C).

Absolute Maximum Ratings

@ Zo=50Ω, T_A= +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2, RF Pulse width = 150 usec, duty cycle = 10%, derated linearly to 0 W at T_{CASE}=+150°C (See note 1)	+62 dBm
RF CW Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2,derated linearly to 0 W at T_{CASE}=+150°C (See note 1)	+56 dBm

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

RFLM-502602QA-TBD Electrical Specifications

@ Z_o=50Ω, T_A= +25°C as measured on the base ground surface of the device.

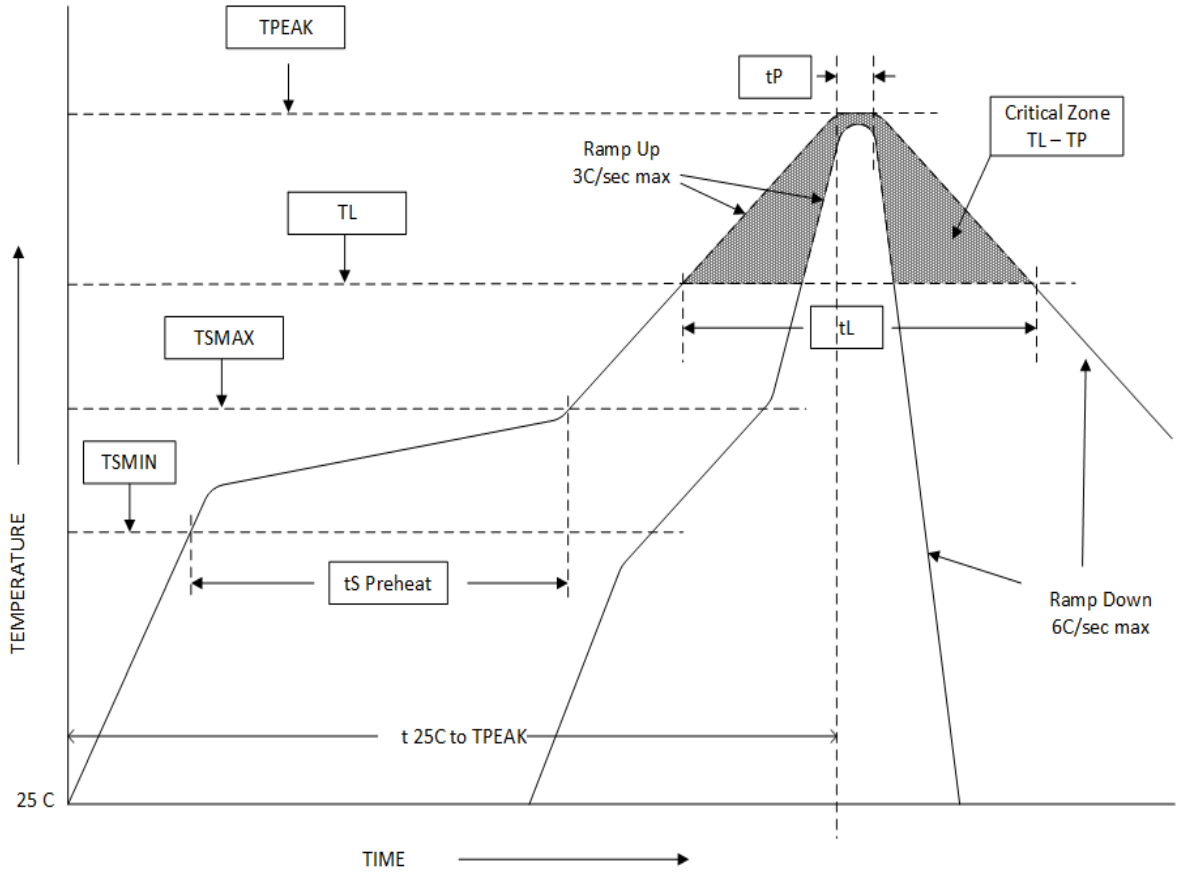
Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	5.0 GHz ≤ F ≤ 6.0 GHz	5.0		6.0	GHz
Insertion Loss	IL	5.0 GHz ≤ F ≤ 6.0 GHz, P_{in}= -20 dBm			1.1	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	5.0 GHz ≤ F ≤ 6.0 GHz, Pin ≤ -20 dBm		0.005		dB/°C
Return Loss	RL	5.0 GHz ≤ F ≤ 6.0 GHz, Pin= -20 dBm	13			dB
Input 1 dB Compression Point	IP_{1dB}	5.0 GHz ≤ F ≤ 6.0 GHz		TBD		dBm
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 150 usec, duty cycle = 10%, t_{rise} ≤ 2us, t_{fall} ≤ 2 usec			62	dBm
CW Incident Power	$Pi_{nc(CW)}$	5.0 GHz ≤ F ≤ 6.0 GHz			50	dBm
Flat Leakage	FL	P_{in} = 62 dBm, RF Pulse width = 150 us, duty cycle = 10%, t_{rise}≤ 2 us, t_{fall}≤ 2 us		21		dBm
Spike Leakage	SL	Pin = 62 dBm, RF Pulse width = 150 us, duty cycle = 5%			0.5	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = 50 dBm peak, RF PW = 150 us, duty cycle = 10%, trise ≤ 2us, t_{fall} ≤ 1 usec			10	usec

Assembly Instructions

The RFLM-502602QA-TBD may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	100°C 150°C 60 – 120 sec	100°C 150°C 60 – 120 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	245°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	183°C 60 to 150 sec	217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFLM-502602QA-TBD Limiter Module Package Outline Drawing

TBD

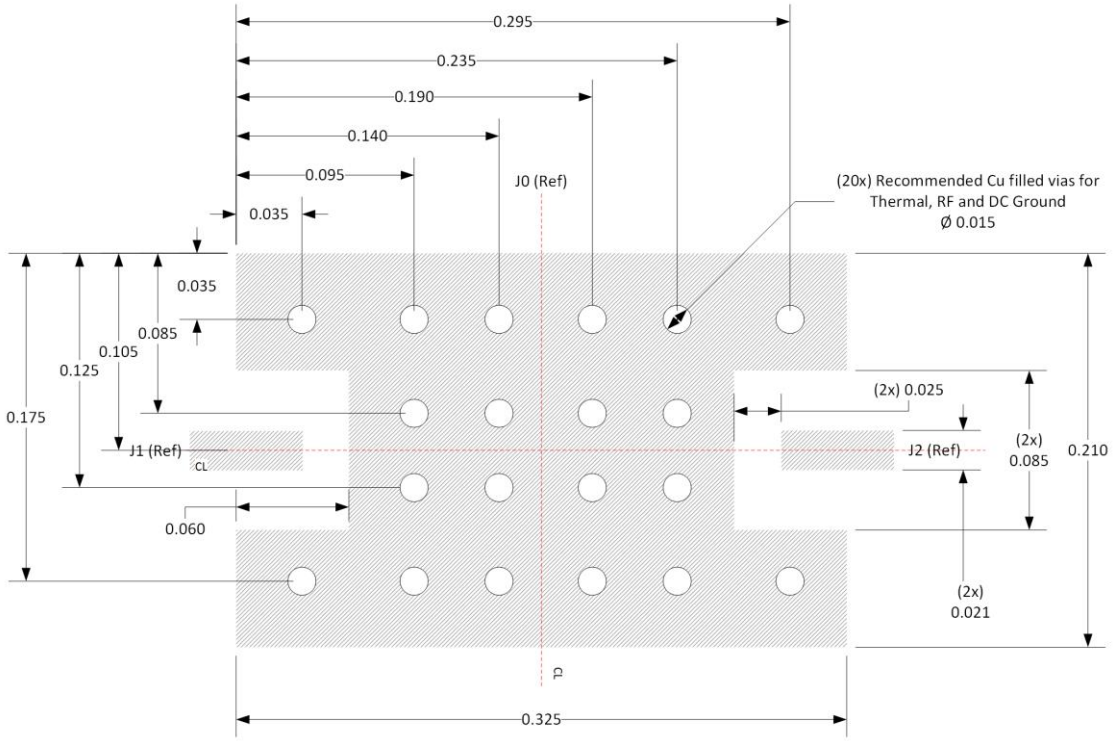
[Either 8mmx5mm or 10mmx6mm]

Notes:

1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (15 u in typ Au plated over Ti-Pd).

Recommended RF Circuit Solder Footprint for the RFLM-502602QA-TBD

[Either 8mmx5mm or 10mmx6mm]



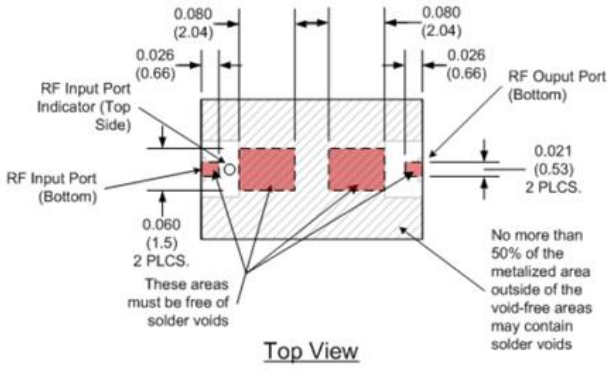
Notes:

1) Recommended PCB material is rogers 4350, 10 mils thick.
2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.

Thermal Design Considerations:

The design of the RFLM-502602QA-TBD family of Limiter Modules permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than +55°C.

There must be a minimal thermal and electrical resistance between the limiter and ground. Adequate thermal management is required to maintain T_{jc} at less than +175°C and thereby will not adversely affect the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.



Dimensions in inches (mm).

Part Number Ordering Detail:

The RFLM-502602QA-TBD Limiter Modules are available in the following shipping format:

Part Number	Description	Packaging
RFLM-502602QA-TBD	5.3 GHz to 5.7 GHz Band Limiter, No DC Blocking Capacitors	Gel-Pack
RFLM-502602QA-TBD HP EVB	RFLM-502602QA-TBD High Power Evaluation Board	Box